Amendments to the Substitute Specification:

Please replace paragraph [0028] with the following amended paragraph:

[0028] In addition, in accordance with the present invention, the depth of said first trenches finally becomes deeper than that of said ~~secqnd second~~ second and third trenches.

Please replace paragraph [0132] with the following amended paragraph:

[0132] Next, as shown in Fig. 12, a gate electrode forming film 9a made of non-doped amorphous silicon, which can be effectively filled in, for example, even into narrow trenches, is deposited through a CVD method, or the like, on the semiconductor substrate 1, including the trenches 7a and 7b, and, after that, this is polished through a CMP method, or the like, as shown in Fig. 13, by using the insulating film 5, made of silicon nitride, or the like, as an etching stopper. Thereby, the unevenness of the surface of the gate electrode forming film 9a due to the difference of the depths of the trenches 7a and 7b can be eliminated. At this stage, the top surface of the gate electrode forming film 9a within the trenches 7a and 7b is at almost an equal height to the top surface of the remaining insulating film 5. Then, since the trench width has become larger within the trenches 7a and 7b due to the etching treatment, or the like, of the above described sacrificial oxide film by hydrofluoric acid, there are some cases where voids are formed in the gate electrode forming film 9a, which is filled in into there; and, therefore, the top part of

the gate electrode forming film 9a is removed through etching by means of an isotropic etching treatment, or the like, until the voids are opened using the insulating film 5 as an etching mask, as shown in Fig. 14. Though it is possible to carry out the removal of the gate electrode forming film 9a until the voids are opened through only etching, the etching proceeds into a gate electrode forming film 9a at the void bottom through this method so that the gate insulating film 8b is exposed therefrom, so as to include the risk of defects. Accordingly, as described in the present embodiment, the step of removing the gate electrode forming film 9a until the voids are opened can be carried out by CMP up to the midway point in the process, and by reducing the etching amount of the gate electrode forming film 9a at the void bottoms ~~can be reduced~~ so as to prevent the occurrence of the above described problem.